C-BAND 10 WATT MMIC AMPLIFIER MANUFACTURED USING REFRACTORY SAG PROCESS

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ABSTRACT

The design and performance of a C-Band single chip GaAs MMIC Amplifier manufactured using the refractory self-aligned gate process is described. The amplifier demonstrates 10 watts power output at 5.5 GHz with associated gain of 5 dB and power added efficiency of 36%. The functional yield of the IC on the best wafer was 70%. To our knowledge, these results exceed the best published results for C-Band power MMIC amplifiers.

INTRODUCTION

There is a great deal of interest in finding more reliable power sources for wideband communication, T/R module and ECM applications. Power MMIC amplifiers look very attractive in terms of cost, light weight, reproducibility and reliability. Many companies have designed high power MMIC amplifiers in order to meet the challenge. During the past decade there has been significant progress in the areas of monolithic power amplifiers covering narrow band and broadband frequency ranges [1-10]. At ITT/GTC we have developed MMIC power amplifiers using a new fully planar, refractory self-aligned gate (SAG) technology [11] demonstrating state-of-the-art performance in a manufacturing environment. This paper reports the design, fabrication and test results of a C-band single chip MMIC power amplifier with 10 W power output.

FET DESIGN AND MODEL

The input impedance level, the heat dissipation, the source inductance, and the phase difference between different parts of the power FET play a significant role in the selection of FET size. In the current design we have used a 4 mm gate periphery FET with a unit finger width of 250 microns as a standard cell. The power MMIC design is based upon measured data for the FET which has three source vias for low parasitic source grounding (0.05 Ω, 0.01 nH for each via typically). The FET has been optimized for maximum power and efficiency at C-band and has 16 fingers. The substrate thickness, 75 μm, is chosen as a compromise between reducing the thermal resistance and being able to design and handle power MMIC's.

The design of power amplifiers is based on an innovative method which has been developed at the ITT Gallium Arsenide Technology Center. The method determines accurate linear type models for power FETs which are used to design matching networks and to simulate accurately the performance of power amplifiers. The method is suitable for single and multistage amplifiers. The models are derived by measuring I-V characteristics, small-signal S-parameters measured at 3%, 25% and 40% of I_{DSS}, and loadpull contour data at the operating drain-source voltage and frequencies. The equivalent circuit of a power FET is shown in Fig. 1, and the element values are given in Table 1.

MMIC DESIGN

In order to meet our objectives of 8 W power output with reasonably good MMIC yield, we selected two single-ended amplifiers whose outputs were combined on a single chip to achieve the high power output. Each of the single-ended amplifiers used a pair of standard 4-mm gate FET compositely acting as an 8-mm FET.

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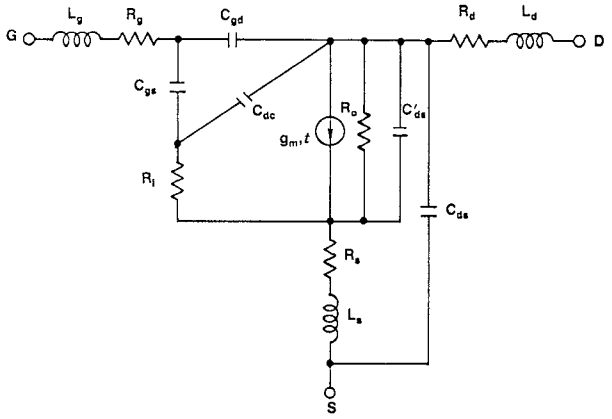

Figure 1 Equivalent circuit model of a power FET.

Table 1 Typical Equivalent Circuit Model Values of a 4-mm FET

L_g (Gate Inductance)	= 0.05 nH
L_s (Source Inductance)	= 0.02 nH
L_d (Drain Inductance)	= 0.05 nH
R_g (Gate Ohmic Resistance)	= 1 Ω
R_s (Source Bulk Resistance)	= 0.4 Ω
R_d (Drain Bulk Resistance)	= 0.4 Ω
R_i (Channel Resistance)	= 0.19 Ω
R_o (Drain to Source Resistance	= 20 Ω
C_{gs} (Gate to Source Capacitance)	= 5 pF
C_{gd} (Gate to Drain Capacitance)	= 0.064 pF
C_{dc} (Dipole Capacitance)	= 0.032 pF
C'_{ds} (Drain to Source Capacitance	= 0.96 pF
C_{ds} (Drain to Ground Capacitance)	= 0.112 pF
g_m (Transconductance)	= 300 mS
t (Transit Time)	= 3 pF

Note: For matchinbg to load line typical R_o = 13 Ω.

Each 8-mm FET is matched to 100 ohm input and output under maximum power output condition. Both distributed and lumped elements were used in the matching networks. The elements of the output matching network were selected for minimum possible loss with a good match as well as to satisfy electromigration requirements. Finally, two of these single ended designs are combined to get 8-W amplifier.

Capacitors, which were used for DC-blocking, RF bypassing and matching were all metal-insulator-metal (MIM) type. The dielectric material used for the capacitor is 2000Å thick Si_3N_4. This provides a capacitance of 300 pF/mm^2 and a breakdown voltage above 30 V. The tolerance in capacitance is ± 5%. Large RF bypass capacitors as well as resistive gate bias were used for amplifier stabilization at low frequency. The drain bias is applied to each FET through a low impedance short circuited λ/4 stub. Figure 2 shows the schematic diagram of the 8-W power amplifier chip.

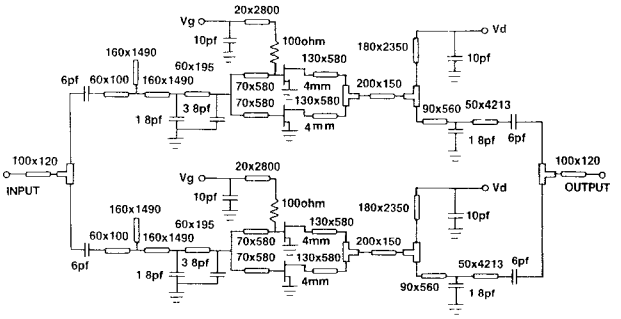

Figure 2 Schematic of a 10W power amplifier. Microstrip dimensions are in μm.

FABRICATION

The power ICs reported in this paper are fabricated using the refractory metal, multifunctional self-aligned gate (MSAG) MMIC process developed at ITT/GTC. The process flow diagram is shown in Fig. 3 and a detailed description of the process is given in reference [11]. The process includes Au/Ge/Ni metallization for ohmic contacts, 0.5 μm TiWN Schottky barrier gates and ion-implanted resistors. The 0.5 μm TiWN gates are covered by a 0.8 μm overlay, after planarization. Silicon nitride is used for both capacitors and passivation. The airbridges, microstrip lines and bonding pads are 5 μm thick plated gold. The wafer is lapped to its final thickness of 75 μm, and backside via holes are then etched and plated. A photograph of the chip is shown in Fig. 4. The measured functional on-wafer yield for 4 wafers in a lot is plotted in Fig. 5. (This is a low-power screening test).

TEST RESULTS

Several 8-W amplifiers were assembled on a 0.5 x 0.5 inch Elkonite (Cu-W) carrier. Elkonite material was chosen for good thermal conductivity and thermal expansion match to GaAs and alumina. Although ICs were fabricated on a thin substrate (75 μm thick) using 18 via-holes, we had no problem in assembling these chips by using gold-tin (AuSn) die attach at 290°C.

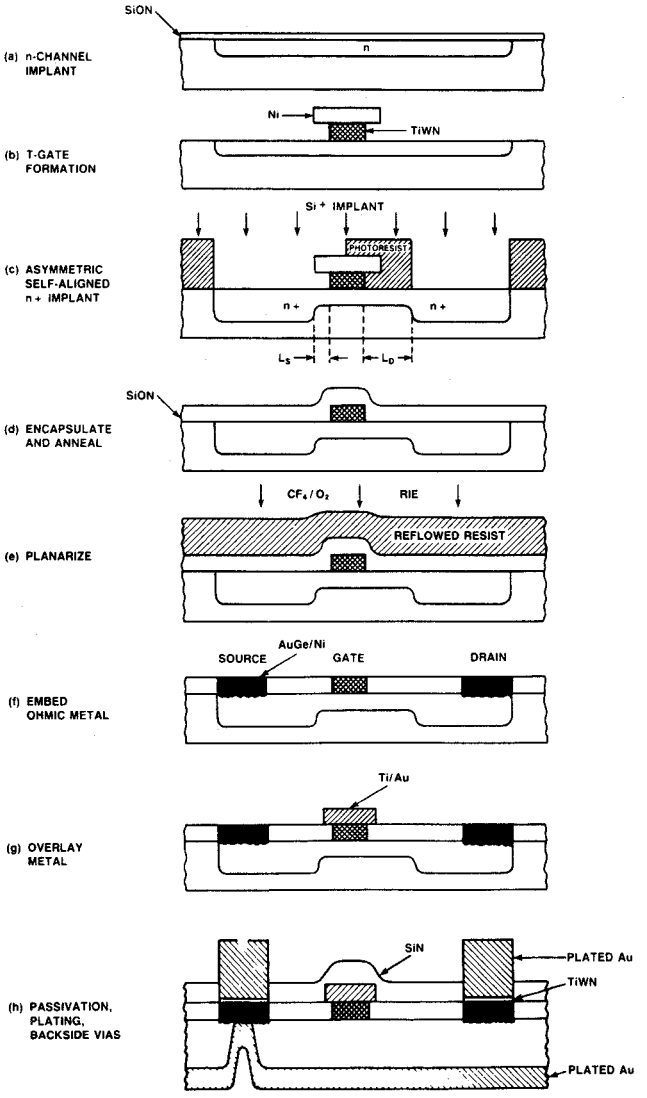

Figure 3 MSAG FET fabrication process flow diagram.

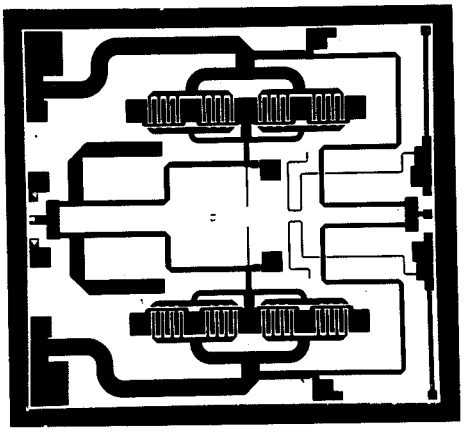

Figure 4 Photograph of a 10W power MMIC (Chip size=4.14x4.48x0.075mm).

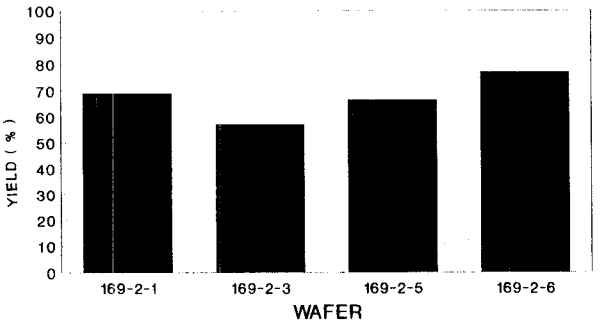

Figure 5 Functional yield of 10W ICs from a lot of 4 wafers.

Typical measured characteristics for the IC are plotted in Fig. 6 as a function of input power at 5.5 GHz. The amplifier has about 6 dB gain, 9 W power output and 37% power added efficiency at the 1-dB gain compression point. At the 2-dB gain compression point the peak power output was 10 W (0.63 W/mm power density) and 36% power added efficiency. Power out as a function of frequency at 1-dB gain compression, is shown in Fig. 7. The gain flatness is $\pm$ 0.5 dB over the 5.2 to 6 GHz frequency range. Table 2 summarizes the measured results for these amplifiers.

CONCLUSIONS

In summary, we developed a C-band 10-W single chip power MMIC amplifier demonstrating state-of-the-art performance. This excellent performance is attributed to accurate model for 4-mm FETs, a new IC design method, simple circuit typology, and high yield and high performance MSAG processing.

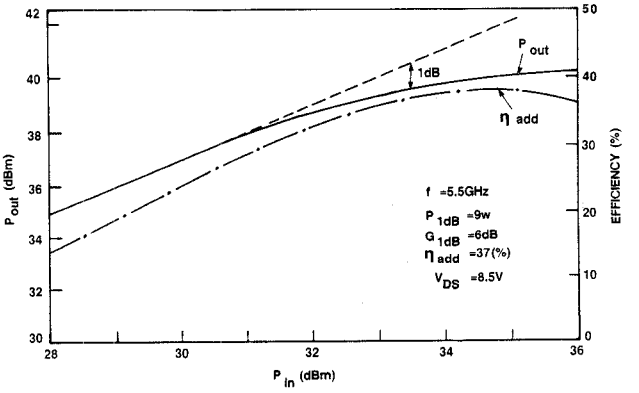

Figure 6 Power output versus power input for a 10W power MMIC.

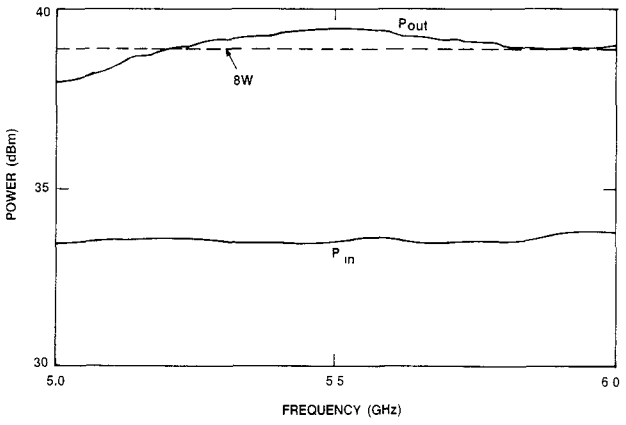

Figure 7 Variation of P_{out} and P_{in} as a function of frequency of a 10W power MMIC.

Table 2 Summary of measured results for 10 W MMIC Amplifiers

Parameter	Goals	Measured
Frequency (GHz)	5.2-5.8	5.2-6.0
P_{1dB} (min)	8.0	8.0
P_{2dB} (min)	8.5	9.0
P_o/mm (W/mm) @P_{2dB}	0.53	0.56
Gain (dB), min. @ P_{1dB}	5.5	5.5
Power Added Efficiency (%), min. @P_{1dB}	30	32
VSWR, Max.	2:1	3:1

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